WHAT IS CLAIMED IS:

1. A semiconductor memory cell comprising:

a plurality of first wiring located along a first direction with a first wiring pitch;

a plurality of vertical transistor formed over said first wiring, which is comprised of source region, drain region, channel region, gate insulating film formed along said channel region and a gate electrode formed on said gate insulating film, wherein said gate electrode is separated from each other along said first direction, but connected from each other along a second direction intersecting at right angle with said first direction;

a plurality of chalcogenide material formed over said drain region; and

a plurality of second wiring connected with said chalcogenide material, and located over said chalcogenide material along said first direction with a second wiring pitch.

2. A semiconductor memory cell according to claim 1, wherein a plug is formed between said first wiring and said source region.

3. A semiconductor memory cell according to claim 1, wherein a barrier film is formed between said chalcogenide material and said drain region.

4. A semiconductor memory cell according to claim 3, wherein said barrier film is one of TiAlN or oxide of TiAlN or WTi, or laminated films of either of TiAlN or oxide of TiAlN or WTi, or ITO .

5. A semiconductor memory cell according to claim 1, wherein an area of said chalcogenide material connected to said drain region is smaller than an area of said drain region.

6. A semiconductor memory cell according to claim 1, wherein a chalcogenide material includes at least antimony and tellurium.

7. A semiconductor memory cell according to claim 1, wherein said first wiring pitch is smaller than said second wiring pitch.

8. A semiconductor memory cell comprising:

a plurality of first wiring located along a first direction with a first wiring pitch;

a plug connected with said first wiring, and formed over said first wiring;

a plurality of vertical transistor formed on said plug, which is comprised of source region, channel region, drain region, gate insulating film formed along said channel region and a gate electrode formed on said gate insulating film, wherein said gate electrode is separated from each other along said first direction, but connected from each other along a second direction intersecting at right angle with said first direction;

a plurality of chalcogenide material formed over said drain region; and

a plurality of second wiring connected with said chalcogenide material, and located over said chalcogenide material along said first direction with a second wiring pitch.

9. A semiconductor memory cell according to claim 8, wherein a barrier film is formed between said chalcogenide material and said drain region.

10. A semiconductor memory cell according to claim 9, wherein said barrier film is one of TiAlN or oxide of TiAlN or WTi, or laminated films of either of TiAlN or oxide of TiAlN or WTi, or ITO.

11. A semiconductor memory cell according to claim 8, wherein a area of said chalcogenide material connected to said drain region is smaller than a area of said drain region.

12. A semiconductor memory cell according to claim 8, wherein a chalcogenide material includes at least antimony and tellurium.

13. A semiconductor memory cell according to claim 8, wherein said first wiring pitch is

smaller than said second wiring pitch.

14. A semiconductor memory cell comprising:

a plurality of first wiring located along a first direction with a first wiring pitch;

a plug connected with said first wiring, and formed over said first wiring;

a plurality of vertical transistor formed on said plug, which is comprised of source region, channel region, drain region, gate insulating film formed along said channel region and a gate electrode formed on said gate insulating film, wherein said gate electrode is separated from each other along said first direction, but connected from each other along a second direction intersecting at right angle with said first direction;

a plurality of chalcogenide material formed over said drain region; and

a plurality of second wiring connected with said chalcogenide material, and located over said chalcogenide material along said first direction with a second wiring pitch which is smaller than said first wiring pitch.

15. A semiconductor memory cell according to claim 14, wherein a barrier film is formed between said chalcogenide material and said drain region.

16. A semiconductor memory cell according to claim 15, wherein said barrier film is one of TiAlN or oxide of TiAlN or WTi, or laminated films of either of TiAlN or oxide of TiAlN or WTi, or ITO.

17. A semiconductor memory cell according to claim 14, wherein an area of said chalcogenide material connected to said drain region is smaller than an area of said drain region.

18. A semiconductor memory cell according to claim 14, wherein a chalcogenide material at least includes antimony and tellurium.